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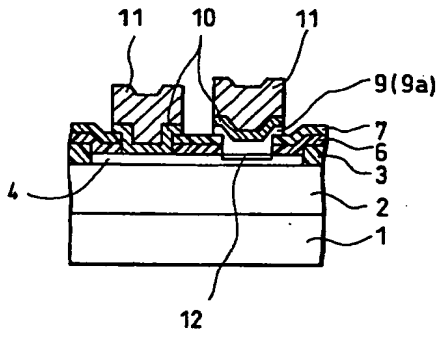
(54) Bipolar transistor and method of fabricating it

(57) The method of fabricating a semiconductor device includes the steps of: (a) forming a first molecular beam epitaxy layer (4) on a semiconductor substrate (1); and (b) forming a second molecular beam epitaxy layer (9) on the first molecular beam epitaxy layer (4), characterized by the step of implanting impurities into the first molecular beam epitaxy layer (4) prior to the step (b). The method makes it possible to establish not only a base region but also an emitter region by ambient temperature growth by means of an MBE apparatus. Herein, the emitter region has a shallow depth and uniform impurities content by implanting antimony into a region with a substrate being applied a voltage directly in an MBE apparatus. It is no longer necessary to carry out thermal treatment at high temperature after the formation of a base region, resulting in prevention of crystallinity degradation and prevention of changes in impurities depth profile.

FIG.3



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Description

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The invention relates to a semiconductor device and a method of fabricating the same, and more particularly to a semiconductor device having layers formed by means of molecular beam epitaxy and a method of fabricating a semiconductor device by using an apparatus for carrying out molecular beam epitaxy.

DESCRIPTION OF THE RELATED ART

Japanese Unexamined Patent Publication No. 5-211158 has suggested a method of fabricating a semiconductor device by means of molecular beam epitaxy (hereinafter, referred to simply as "MBE"). Hereinbelow is explained the method with reference to Figs. 1A to 1D.

First, as illustrated in Fig. 1A, there is formed an N^- epitaxial layer 2 over an N-type silicon substrate 1. The N^- epitaxial layer 2 has a thickness ranging from 0.8 to 1.3 μm, and a resistivity ranging from 0.5 to 1.0 Ω-cm. Then, the N^- epitaxial layer 2 is thermally oxidized to thereby form a silicon dioxide film 3 having a thickness of about 100 nm. Then, a part of the silicon dioxide film 3 is removed by photolithography and anisotropic etching to thereby form a base region. Then, silicon and boron are evaporated in an apparatus for carrying out molecular beam epitaxy (hereinafter, referred to simply as "MBE apparatus") which provides about 10^{-8} Torr vacuum to thereby form a P-type layer 4 on the N^- epitaxial layer 2 at 650 °C of growth temperature. The P-type layer 4 has a thickness in the range of 30 to 50 nm, and a carrier concentration on the order of 10^{18} cm^{-3}. Hereinbelow, an layer formed by means of the MBE apparatus, including the P-type layer 4, is referred to as "an MBE layer"

Then, silicon and boron are evaporated again in the MBE apparatus to thereby form a P^- MBE layer 5 over the P-type MBE layer 4 at 650 °C of growth temperature. The P^- MBE layer 5 has a thickness in the range of 5 to 20 nm. The P^- MBE layer 5 functions as a buffer layer for maintaining both crystallinity at an interface between an emitter and a base and p-n junction in well condition. Thereafter, polysilicon having grown on the silicon dioxide film 3 are removed by means of photolithography and anisotropic etching such as CF_4 gas etching.

Then, as illustrated in Fig. 1B, a silicon dioxide film 6 and further a silicon nitride film 7 are formed on the P^- MBE layer 5 and the silicon dioxide film 3 by chemical vapor deposition (CVD). The silicon dioxide film 6 and the silicon nitride film 7 both have a thickness of about 100 nm. Then, a photoresist 8 is deposited over the silicon nitride film 7, and patterned by photolithography, followed by anisotropic etching to thereby open an emitter region E.

Then, as illustrated in Fig. 1C, silicon and antimony are evaporated in the MBE apparatus to thereby deposit heavily doped amorphous silicon on the silicon substrate 1 at room temperature, followed by solid phase epitaxy at growth temperature of 730 °C to thereby form an N^+ MBE layer 9 having a thickness in the range of 100 to 200 nm. Then, photolithography and subsequently anisotropic etching such as (CF_4+O_2) gas etching are carried out to the N^+ MBE layer 9 to thereby form an emitter contact 9a.

The thus obtained emitter contact 9a composed of the N^+ MBE layer 9 has been already sufficiently activated. Thus, it is no longer necessary to carry out thermal annealing at high temperature above growth temperature, resulting in that impurities depth profile is scarcely varied, and that it is possible to obtain desired characteristics by controlling thickness of base and emitter and/or carrier concentration.

Thereafter, the photoresist 8 is patterned by photolithography and anisotropically etched to thereby open a base contact B.

Then, as illustrated in Fig. 1D, a titanium (Ti)/platinum (Pt) layer 10 is deposited all over a resultant by vacuum evaporation. A gold layer 11 is deposited on the Ti/Pt layer 10, and then patterned by photolithography. The Ti/Pt layer 10 is anisotropically etched using the patterned gold layer 11 as a mask, to thereby form electrodes of base and emitter of a silicon bipolar transistor.

The above mentioned conventional method has an advantage that an emitter region almost free of crystal defects can be obtained without carrying out thermal annealing at high temperature for activation, because the thin base layer 4 is grown by MBE, and further the N^+ MBE layer 9 is grown through solid phase epitaxy process by means of the MBE apparatus. To the contrary, the above mentioned conventional method has many shortcomings.

First, the emitter region is insufficiently shallow in depth, because the emitter region is established only through annealing in solid phase epitaxy.

Secondly, since a diffusion coefficient of boron in the base layer is greater than a diffusion coefficient of antimony in an emitter, a p-n junction interfacial plane between an emitter and a base is almost equal to an epi-poly interfacial plane established through the solid phase epitaxy. As a result, it is impossible to obtain sufficient crystallinity, which causes a base leakage current to be increased, thereby DC characteristic being deteriorated at a low current. As one of evidences for such deterioration, Fig. 2 shows Gummel plots for a transistor fabricated in accordance with the above mentioned conventional method. It is understood in view of the two curves I_C and I_B in Fig. 2 that a base current IB is greater than a collector current Ic in the range where a current is small, resulting in that the forward current gain linearity is deteriorated.

Thirdly, a rapid thermal annealing (RTA) apparatus may be used in the conventional method to carry out

implantation for forming a shallow emitter region. However, annealing is carried out in so short period of time that temperature in a wafer is not uniformized. As a result, there is generated dispersion in characteristics, which lowers a production yield.

Ion implantation and thermal diffusion, which have been widely used, have a shortcoming that they make the implantation depth so deep that crystal defects are increased, resulting in that it is necessary to carry out thermal annealing at high temperature for activation. In addition, those prior methods have another shortcoming that a silicon wafer has to be taken out of an MBE apparatus each time when ion implantation is to be carried out.

A report No. 27a-T-9 by the title of "B and Sb Heavy Doping for Si-MBE" in the 51st Applied Physical Society lecture meeting, Vol. 1, pp 239, Autumn 1990, has indicated has indicated a problem that it is impossible in conventional methods of fabricating a bipolar transistor to have steep impurities depth profile, because base and emitter are formed by ion implantation and thermal treatment at high temperature such as annealing. Recently, Si-MBE has been applied to formation of a thin base layer for establishing steep impurities depth profile at ambient temperature. However, technique for heavily doping B and Sb is not established yet. Thus, the results of the experiments are reported about activation rate, crystallinity, and dependency on azimuth of substrate planes during B and Sb are being heavily doped.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor device and a method of fabricating the same which are capable of forming an emitter region which are shallow, but sufficiently uniform in impurities concentration with the result of no necessity of thermal annealing at high temperature after the formation of a base layer, prevention of degradation of crystallinity, and prevention of variation of impurities depth profile.

In one aspect, there is provided a method of fabricating a semiconductor device, comprising the steps of: (a) forming a first molecular beam epitaxy layer on a semiconductor substrate; and (b) forming a second molecular beam epitaxy layer on the first molecular beam epitaxy layer, characterized by the step of: (c) implanting impurities into the first molecular beam epitaxy layer prior to the step (b).

It is preferable for the method to further include the steps of: (d) forming a heavily doped first conductivity type layer buried in the semiconductor substrate, the semiconductor substrate having a second conductivity type; (e) forming a lightly doped first conductivity type epitaxial layer on the heavily doped first conductivity type layer so that the lightly doped first conductivity type epitaxial layer is exposed to a surface of the semiconductor substrate; and (f) forming a heavily doped first conductivity type connection layer for connecting the heavily doped first conductivity type layer to a surface of the semiconductor substrate. The steps (d), (e) and (f) are to be carried out in sequence prior to the step (a). The first molecular beam epitaxy layer is formed on the lightly doped first conductivity type epitaxial layer. The second molecular beam epitaxy layer is formed on both the connection layer and a part of the first molecular beam epitaxy layer into which the impurities are implanted. The second molecular beam epitaxy layer is designed to be of a first conductivity type.

It is preferable that the second molecular beam epitaxy layer is formed only on a portion of the first molecular beam epitaxy layer into which the impurities have been implanted. The first molecular beam epitaxy layer may be designed to have an opposite conductivity to that of the semiconductor substrate, and the second molecular beam epitaxy layer may have the same conductivity as that of the semiconductor substrate.

For instance, the first molecular beam epitaxy layer may be comprised of a first epitaxial layer and the second molecular beam epitaxy layer may be comprised of an amorphous layer. The method may further include the step of causing the second molecular beam epitaxy layer to grow in solid phase to a second epitaxial layer and a polysilicon layer.

There is further provided a method of fabricating a semiconductor device, comprising the steps of: (a) forming a first conductivity type epitaxial layer on a second conductivity type semiconductor substrate; and (b) forming a second conductivity type layer on the first conductivity type epitaxial layer, characterized by the steps of: (c) implanting second conductivity type impurities into at least a part of the first conductivity type epitaxial layer, the second conductivity type layer being formed on the part of the first conductivity type epitaxial layer into which the second conductivity type impurities have been implanted; and (d) causing the second conductivity type layer to grow in solid phase, the second conductivity type layer being an amorphous layer.

It is preferable for the method to further include the steps of: (e) forming a heavily doped second conductivity type layer buried in the semiconductor substrate; (f) forming a lightly doped second conductivity type epitaxial layer on the heavily doped second conductivity type layer so that the lightly doped second conductivity type epitaxial layer is exposed to a surface of the semiconductor substrate; (g) forming a heavily doped second conductivity type connection layer for connecting the heavily doped second conductivity type layer to a surface of the semiconductor substrate. The steps (e), (f) and (g) are to be carried out in sequence prior to the step (a).

There is still further provided a method of fabricating a semiconductor device, comprising the steps of: (a) forming a first conductivity type base region in a second conductivity type collector region by molecular beam epitaxy; and (b) forming a second conductivity type layer on the first conductivity type base region by molecular beam epitaxy, characterized by the steps of: (c)

forming an emitter region in the base region by implanting second conductivity type impurities into the base region by molecular beam epitaxy, the second conductivity type layer being formed on the emitter region, the second conductivity type layer being formed of an amorphous layer; and (d) forming an emitter contact region by causing the second conductivity type amorphous layer to grow in solid phase.

It is preferable for the method to further include (e) forming a heavily doped second conductivity type layer buried in a first conductivity type semiconductor substrate; (f) forming a lightly doped second conductivity type epitaxial layer on the heavily doped second conductivity type layer so that the lightly doped second conductivity type epitaxial layer is exposed to a surface of the semiconductor substrate; and (g) forming a heavily doped second conductivity type connection layer for connecting the heavily doped second conductivity type layer to a surface of the semiconductor substrate. The steps (e), (f) and (g) are to be carried out in sequence prior to the step (a). The second conductivity type layer is formed also on the connection layer.

The steps where molecular beam epitaxy is to be accomplished may be carried out in a common apparatus for accomplishing molecular beam epitaxy. The impurities are selected from antimony (Sb), phosphorus (P) and arsenic (As). Impurities implantation is accomplished by application of a voltage directly to the semiconductor substrate during doping.

In another aspect, there is provided a semiconductor device comprising: (a) a first conductivity type semiconductor substrate; (b) a first molecular beam epitaxy layer formed on the semiconductor substrate, the first molecular beam epitaxy layer being of a second conductivity type; and (c) a second molecular beam epitaxy layer formed on the impurities implantation layer, the second molecular beam epitaxy layer being of a first conductivity type, characterized by the step of: (d) an impurities implantation layer into which first conductivity type impurities are implanted, formed at a surface of the first molecular beam epitaxy layer.

It is preferable for the semiconductor device to further include (e) a heavily doped first conductivity type layer buried in the semiconductor substrate; (f) a lightly doped first conductivity type epitaxial layer formed on the heavily doped first conductivity type layer so that the lightly doped first conductivity type epitaxial layer is exposed to a surface of the semiconductor substrate; and (g) a heavily doped first conductivity type connection layer for connecting the heavily doped first conductivity type layer to a surface of the semiconductor substrate. The second molecular beam epitaxy layer is formed also on the connection layer.

The first molecular beam epitaxy layer may be comprised of an epitaxial layer, and the second molecular beam epitaxy layer may be comprised of an amorphous layer. For instance, the impurities are selected from antimony (Sb), phosphorus (Pb) and arsenic (As).

There is further provided a semiconductor device comprising: (a) a first conductivity type semiconductor substrate; (b) a second conductivity type epitaxial layer formed on the semiconductor substrate; and (c) a first conductivity type layer formed on the second conductivity type epitaxial layer, characterized by: (d) an impurities implantation layer comprised of a part of the second conductivity type epitaxial layer into which first conductivity type impurities are implanted. The first conductivity type layer is formed on the impurities implantation layer, and is comprised of an amorphous layer.

It is preferable for the semiconductor device to further include: (e) a heavily doped first conductivity type layer buried in the semiconductor substrate; (f) a lightly doped first conductivity type epitaxial layer formed on the heavily doped first conductivity type layer so that the lightly doped first conductivity type epitaxial layer is exposed to a surface of the semiconductor substrate; and (g) a heavily doped first conductivity type connection layer for connecting the heavily doped first conductivity type layer to a surface of the semiconductor substrate. The first conductivity type layer is formed also on the connection layer, and is comprised of an amorphous layer.

There is still further provided a semiconductor device comprising: (a) a first conductivity type semiconductor substrate; (b) a second conductivity type base region formed in a first conductivity type collector region of the semiconductor substrate; and (c) a first conductivity type layer formed on the emitter region, characterized by: (d) an emitter region formed in the base region, first conductivity type impurities being implanted into the emitter region.

It is preferable for the semiconductor device to further include: (e) a heavily doped first conductivity type layer buried in the semiconductor substrate; (f) a lightly doped first conductivity type epitaxial layer formed on the heavily doped first conductivity type layer so that the lightly doped first conductivity type epitaxial layer is exposed to a surface of the semiconductor substrate; and (g) a heavily doped first conductivity type connection layer for connecting the heavily doped first conductivity type layer to a surface of the semiconductor substrate. The first conductivity type layer is formed also on the connection layer, and is comprised of an amorphous layer.

In accordance with the above mentioned present invention, it is possible to establish not only a base region but also an emitter region in ambient temperature growth by means of an MBE apparatus. Herein, the emitter region can have a shallow depth and a uniform, sufficient impurities content by implanting impurities such as antimony (Sb) into a region with a substrate being DC-biased in an MBE apparatus. Thus, it is no longer necessary to carry out thermal treatment at high temperature after the formation of a base region, resulting in prevention of degradation of crystallinity and prevention of changes in impurities depth profile. In addition, since a p-n junction interfacial plane is formed in a base epitaxial layer, it is possible to obtain better

crystallinity with the result of improvement in DC characteristic.

The above and other objects and advantageous features of the present invention will be made apparent from the following description made with reference to the accompanying drawings, in which like reference characters designate the same or similar parts throughout the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A to 1D are cross-sectional views of a silicon bipolar transistor, each illustrating respective step of a conventional method of fabricating a silicon bipolar transistor.

Fig. 2 shows Gummel plots for a conventional silicon bipolar transistor.

Fig. 3 is a cross-sectional view of a silicon bipolar transistor fabricated in accordance with the first embodiment of the present invention.

Figs. 4A to 4G are cross-sectional views of a silicon bipolar transistor fabricated in accordance with the first embodiment of the present invention, each illustrating respective step of a method of fabricating the same.

Fig. 5 shows Gummel plots for a silicon bipolar transistor fabricated in accordance with the first embodiment of the present invention.

Fig. 6 is a cross-sectional view of a silicon bipolar transistor fabricated in accordance with the second embodiment of the present invention.

Figs. 7A to 7D are cross-sectional views of a silicon bipolar transistor fabricated in accordance with the second embodiment of the present invention, each illustrating respective step of a method of fabricating the same.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 3 is a cross-sectional view of a silicon bipolar transistor fabricated in accordance with the first embodiment of the present invention. The illustrated silicon bipolar transistor includes a N-type silicon substrate 1 in which an N^- epitaxial layer 2 is formed. On the N^- epitaxial layer 2 are formed silicon dioxide films 3 between which a device formation region is formed. On the N^- epitaxial layer 2 and between the silicon dioxide films 3 is deposited a P-type MBE layer formed by means of molecular beam epitaxy. Impurities such as antimony (Sb) are implanted into a part of the P-type MBE layer 4 to thereby form an impurities implantation layer 12 at a surface of the P-type MBE layer 4.

On the N^- epitaxial layer 2 and the silicon dioxide films 3 are deposited a silicon dioxide film 6 and a silicon nitride film 7. The silicon dioxide film 6 and silicon nitride film 7 are etched out to thereby form two openings, one of which forms an emitter region in alignment with the impurities implantation layer 12, and the other forms a base region.

In the emitter region, an N^+ MBE layer 9 is deposited on the impurities implantation layer 12 by molecular beam epitaxy to thereby form an emitter contact 9a. On the emitter contact 9a are formed a patterned titanium (Ti)/platinum (Pt) layer 10 and a patterned gold layer 11. In the base region, on the P-type MBE layer 4 are formed the patterned Ti/Pt layer 10 and gold layer 11.

A method of fabricating the silicon bipolar transistor illustrated in Fig. 3 is explained hereinbelow with reference to Figs. 4A to 4G.

First, as illustrated in Fig. 4A, there is formed an N^- epitaxial layer 2 in an N-type silicon substrate 1. The N^- epitaxial layer 2 has a thickness ranging from 0.8 to 1.3 μm, and a resistivity ranging from 0.5 to 1.0 Ω-cm. Then, the N^- epitaxial layer 2 is thermally oxidized to thereby form a silicon dioxide film 3 having a thickness of about 100 nm. Then, a part of the silicon dioxide film 3 is removed by photolithography and anisotropic etching to thereby form a base region. Then, silicon and boron are evaporated in an MBE apparatus which provides about 10^{-8} Torr vacuum, to thereby form a P-type layer 4 on the N^- epitaxial layer 2 at 650 °C of growth temperature. The P-type layer 4 has a thickness in the range of 30 to 50 nm, and a carrier concentration on the order of 10^{18} cm^{-3}. There may be formed a P^- MBE layer on the P-type layer 4 by evaporating silicon and boron in the MBE apparatus and growing the layer at 650 °C of growth temperature. The P^- MBE layer may have a thickness in the range of 5 to 20 nm. The growth temperature is determined in dependence on plane azimuth of a substrate. In general, the growth is continued for a couple of minutes at temperature in the range of 620 °C to 700 °C.

Thereafter, polysilicon having grown on the silicon dioxide films 3 are removed by means of photolithography and anisotropic etching such as CF_4 gas etching.

Then, as illustrated in Fig. 4B, a silicon dioxide film 6 and further a silicon nitride film 7 are formed on the P-type MBE layer 5 and the silicon dioxide films 3 by chemical vapor deposition (CVD). The silicon dioxide film 6 and the silicon nitride film 7 both have a thickness of about 100 nm. Then, a photoresist 8 is deposited over the silicon nitride film 7, and patterned by photolithography, followed by anisotropic etching to thereby open an emitter region E.

After removal of the photoresist 8, antimony (Sb) ions are implanted to a resultant from knudsen cells equipped with the MBE apparatus, as illustrated in Fig. 4C. During Sb ions implantation, a voltage is applied to the silicon substrate 1 in the range of -1 to -3 kV in the MBE apparatus. The DC bias facilitates ionized Sb atoms to be implanted into the P-type MBE layer 4, resulting in that a shallow N^+ Sb implantation layer 12 is formed in the P-type MBE layer 4. The Sb atoms are implanted into the P-type MBE layer 4 at a dose of 1×10^{19} to 10^{20} atoms/cm^3 at a depth in the range of 5 to 20 nm.

As an alternative to Sb atoms, phosphorus (P) or arsenic (As) atoms may be implanted into the P-type MBE layer 4. However, phosphorus is likely to burn in

atmosphere, and arsenic is like to contaminate the MBE apparatus. In addition, atoms having a heavy atomic weight such as P and As have a shortcoming that they are likely to be implanted too deep. Since antimony atoms have a small atomic weight, it is possible to control them so that they are implanted into the P-type MBE layer 4 at a shallow depth. Thus, it is most preferable to use antimony as impurities. An implantation depth of antimony atoms is about tens of nanometers at greatest, which cannot be accomplished by usual ion implantation.

As used herein, the term "MBE apparatus" indicates an apparatus for forming a thin film by epitaxial growth, in particular, gas phase epitaxy, in further particular, physical deposition. In the MBE apparatus, composition elements are transformed into molecular beam in the form of beam under ultra-high vacuum, and then the beam is irradiated to a substrate to thereby carry out epitaxy. The growth rate is so small that it is relatively easy to form a thin film. It is also possible to form an epitaxial layer having good crystallinity by thermal treatment at low temperature.

A lot of ionized atoms exist in the molecular beam in the MBE apparatus. These ionized atoms are implanted into the silicon substrate at a shallow depth by directly DC-biasing the silicon substrate in the MBE apparatus. This process gives little damage to the substrate, and makes it possible to activate those ionized atoms with thermal treatment even at low temperature.

Then, as illustrated in Fig. 4D, heavily doped amorphous silicon is deposited on the silicon nitride film 7 and the Sb implantation layer 12 at room temperature by evaporating silicon and antimony in the MBE apparatus, followed by carrying out solid phase epitaxy process at growth temperature of 730 °C to thereby form an N^+ MBE layer 9 having a thickness in the range of 100 to 200 nm. The Sb implantation layer 12 is activated simultaneously with the formation of the N^+ MBE layer 9 to thereby establish an emitter region E.

The conditions for growth of the N^+ MBE layer 9 are follows.

Growth temperature: 720 °C to 750 °C
Annealing time: 3 to 5 minutes

A layer formed by solid phase epitaxy process can have less crystal defects than a layer formed by other processes. Since there are much generated crystal defects in a layer formed by widely used usual ion implantation process, it is necessary to thermally treat the layer at high temperature for activation in the usual ion implantation. On the other hand, the ion implantation to be carried out with a silicon substrate being DC-biased in the MBE apparatus needs less energy for implantation than the usual ion implantation. Thus, the silicon substrate is less damaged, and hence can be sufficiently activated even at low temperature, resulting in that it is no longer necessary in the embodiment to thermally treat the substrate at high temperature. In addition, since it is possible to carry out a series of fabrication steps in an MBE apparatus, time and cost for fabrication can be significantly saved.

Thereafter, as illustrated in Fig. 4E, a photoresist 8 is deposited over the N^+ MBE layer 9 and patterned by photolithography, and then etched by anisotropic etching such as (CF_4+O_2) gas etching to thereby form an emitter contact 9a. The thus formed emitter contact 9a made of the N^+ MBE layer 9 has been already sufficiently activated.

Then, after removal of the photoresist 8 deposited on the emitter contact 9a, a photoresist 8 is deposited again over a resultant, and patterned by photolithography. Then, as illustrated in Fig. 4F, the photoresist 8 is anisotropically etched to thereby open a base contact B.

Then, after removal of the photoresist 8, as illustrated in Fig. 4G, a titanium (Ti)/platinum (Pt) layer 10 is deposited all over a resultant by vacuum evaporation. A gold layer 11 is deposited on the Ti/Pt layer 10, and then patterned by lithography. The Ti/Pt layer 10 is anisotropically etched using the patterned gold layer 11 as a mask, to thereby form electrodes of base and emitter of the silicon bipolar transistor.

In the above mentioned embodiment, not only a base but also an emitter are grown in an MBE apparatus, and impurities such as antimony (Sb) are implanted into a substrate at a shallow depth with the substrate being DC-biased in the MBE apparatus. Thus, unlike the conventional methods, a p-n junction interfacial plane is formed in a base epitaxial layer, and hence, it is possible to form an emitter region having a shallow depth and sufficient impurities concentration with the result of prevention of deterioration of DC characteristic. This is because epitaxial phase and polysilicon phase are not uniform in the vicinity of an interface between them in an emitter region due to solid phase diffusion, but a uniform p-n junction interface can be formed in a base epitaxial layer.

Fig. 5 shows Gummel plots for a transistor fabricated in accordance with the above mentioned embodiment. It is understood in view of Fig. 5 that a base current I_B is smaller than conventional one shown in Fig. 2 at a low current region (axis of ordinate). As a result, it is understood that the forward current gain linearity is improved.

In the above embodiment, if germanium (Ge) is evaporated from another knudsen cell in the MBE apparatus at an appropriate growth rate together with silicon and boron when the P^+ MBE layer 4 is to be formed, it makes a SiGe heterojunction-bipolar transistor.

Hereinbelow is described the second embodiment of the present invention with reference to Fig. 6. Fig. 6 illustrates an integrated circuit including a silicon bipolar transistor fabricated in accordance with the second embodiment of the present invention.

The illustrated silicon bipolar transistor includes a P-type silicon substrate 21 in which there is formed an N^+ buried layer 22. The N^+ buried layer 22 is formed by implanting impurities such as arsenic (As) and antimony

(Sb) into the P-type silicon substrate 21. On the N^+ buried layer 22 is formed an N^- epitaxial layer 2 having a thickness ranging from 0.8 to 1.3 μm and resistivity ranging from 0.5 to 1.0 Ω • cm. There is further formed a N^+ connection layer 23 vertically extending throughout the N^- epitaxial layer 2 for connecting the N^+ buried layer 22 to an N^+ MBE layer 9 formed on a surface of the P-type silicon substrate 1.

As illustrated in Fig. 6 at the left half, on the N^- epitaxial layer 2 are formed base and emitter electrodes which are the same as those of the first embodiment described with reference to in Figs. 3 and 4A to 4G. On the N^+ connection layer 23 is formed a collector electrode having the same structure as that of the emitter electrode. Namely, the collector electrode includes the N^+ MBE layer 9 formed directly on the N^+ connection layer 23, the Ti/Pt layer 10 formed on the N^+ MBE layer 9, and the gold layer 11 formed on the Ti/Pt layer 10.

Hereinbelow is explained, with reference to Figs. 7A to 7D, a method of fabricating the silicon bipolar transistor illustrated in Fig. 6.

First, a photoresist (not illustrated) is deposited all over the P-type silicon substrate 21, and then patterned by photolithography and anisotropic etching so that the photoresist does not exist on a region where the N^+ buried layer 22 is to be formed. Then, as illustrated in Fig. 7A, impurities such as arsenic (As) are implanted into the P-type silicon substrate 21 to thereby form the N^+ buried layer 22.

Then, as illustrated in Fig. 7B, the N^- epitaxial layer 2 is epitaxially grown on the N^+ buried layer 22 by chemical vapor deposition.

Then, as illustrated in Fig. 7C, a photoresist 25 is deposited over the silicon substrate 21 and patterned so that a collector region is open. Thereafter, impurities such as phosphorus (P) is implanted into the silicon substrate 21.

Thus, as illustrated in Fig. 7D, the N^+ connection layer 23 is formed extending through the N^- epitaxial layer 2 for connecting the N^+ buried layer 22 to a later formed collector electrode.

Then, the base and emitter electrodes are formed in the same manner as the first embodiment described with reference to Figs. 4A to 4G. A collector electrode is also formed on the N^+ connection layer 23 in the same manner as the emitter electrode. Thus, there is obtained a silicon bipolar transistor as illustrated in Fig. 6.

By using the P-type silicon substrate 21, the N^+ buried layer 22, and the N^- epitaxial layer 2 as illustrated in Fig. 6, it is possible to fabricate an integrated circuit which is capable of forming a collector contact on an upper surface of the silicon substrate with the base and emitter electrode remaining as they are in the first embodiment illustrated in Fig. 3. It should be noted that LOCOS or trench structure is necessary to be taken in the second embodiment for device isolation. In addition, if a collector contact is made open simultaneously when an emitter contact is made open, it is possible to establish a collector contact, as well as an emitter contact, from heavily doped amorphous silicon into which antimony is implanted in the MBE apparatus, by means of solid phase epitaxy process at growth temperature of 730 °C.

In accordance with the second embodiment, it is possible to form base, emitter and collector contacts directly on an upper surface of a substrate, and thus the silicon bipolar transistor fabricated in accordance with the present invention is applicable to various integrated circuits such as Bi-CMOS.

Similarly to the first embodiment, it is possible also in the second embodiment to fabricate an integrated circuit including a SiGe heterojunction-bipolar transistor by evaporating germanium at an appropriate growth rate together with silicon and boron when the P^+ MBE layer 4 is formed in the MBE apparatus.

The application of the present invention is not to be limited to a bipolar transistor. The present invention can be applied to a thyrister and other semiconductor devices. It is possible to use a semiconductor substrate other than a silicon substrate. In addition, P- and N-type conductivity may be replaced with each other in the above mentioned two embodiments.

Claims

1: A method of fabricating a semiconductor device, comprising the steps of:

(a) forming a first molecular beam epitaxy layer (4) on a semiconductor substrate (1); and (b) forming a second molecular beam epitaxy layer (9) on the first molecular beam epitaxy layer (4), characterized by the step of:
(c) implanting impurities into the first molecular beam epitaxy layer (4) prior to the step (b).

2. The method as set forth in claim 1 further comprising the steps of:

(d) forming a heavily doped first conductivity type layer (22) buried in the semiconductor substrate (21), the semiconductor substrate (21) having a second conductivity type;
(e) forming a lightly doped first conductivity type epitaxial layer (2) on the heavily doped first conductivity type layer (22) so that the lightly doped first conductivity type epitaxial layer (2) is exposed to a surface of the semiconductor substrate (21); and
(f) forming a heavily doped first conductivity type connection layer (23) for connecting the heavily doped first conductivity type layer (22) to a surface of the semiconductor substrate (21),

the steps (d), (e) and (f) being to be carried out in sequence prior to the step (a),

the first molecular beam epitaxy layer (4) being formed on the lightly doped first conductivity type epitaxial layer (2), the first molecular beam epitaxy layer (4) being of a second conductivity type, the impurities being of a first conductivity type,

the second molecular beam epitaxy layer (9) being formed on both the connection layer (23) and a part of the first molecular beam epitaxy layer (4) into which the impurities are implanted, the second molecular beam epitaxy layer (9) being of a first conductivity type.

3. The method as set forth in claim 1, wherein the second molecular beam epitaxy layer (9) is formed only on a portion of the first molecular beam epitaxy layer (4) into which the impurities have been implanted.

4. The method as set forth in claim 1 or 2, wherein the steps (a) and (c) are carried out in a common apparatus for accomplishing molecular beam epitaxy.

5. The method as set forth in any one of claims 1 to 3, wherein the semiconductor substrate (1, 21) is DC-biased during the step (c).

6. The method as set forth in claim 1, wherein the first molecular beam epitaxy layer (4) has an opposite conductivity to that of the semiconductor substrate (1), and the second molecular beam epitaxy layer (9) has the same conductivity as that of the semiconductor substrate (1).

7. A method of fabricating a semiconductor device, comprising the steps of: (a) forming a first conductivity type epitaxial layer (4) on a second conductivity type semiconductor substrate (1); and (b) forming a second conductivity type layer (9) on the first conductivity type epitaxial layer (4), characterized by the steps of:

(c) implanting second conductivity type impurities into at least a part of the first conductivity type epitaxial layer (4), the second conductivity type layer (9) being formed on the part of the first conductivity type epitaxial layer (4) into which the second conductivity type impurities have been implanted; and
(d) causing the second conductivity type layer (9) to grow in solid phase, the second conductivity type layer (9) being an amorphous layer.

8. The method as set forth in claim 7 further comprising the steps of:

(e) forming a heavily doped second conductivity type layer (22) buried in the semiconductor substrate (21);

(f) forming a lightly doped second conductivity type epitaxial layer (2) on the heavily doped second conductivity type layer (22) so that the lightly doped second conductivity type epitaxial layer (2) is exposed to a surface of the semiconductor substrate (21);

(g) forming a heavily doped second conductivity type connection layer (23) for connecting the heavily doped second conductivity type layer (22) to a surface of the semiconductor substrate (21),

the steps (e), (f) and (g) being to be carried out in sequence prior to the step (a).

9. The method as set forth in claim 7 or 8, wherein the semiconductor substrate (1, 21) is DC-biased during the step (c).

10. A method of fabricating a semiconductor device, comprising the steps of: (a) forming a first conductivity type base region in a second conductivity type collector region by molecular beam epitaxy; and (b) forming a second conductivity type layer (9) on the first conductivity type base region by molecular beam epitaxy, characterized by the steps of:

(c) forming an emitter region in the base region by implanting second conductivity type impurities into the base region by molecular beam epitaxy, the second conductivity type layer (9) being formed on the emitter region, the second conductivity type layer (9) being formed of an amorphous layer; and
(d) forming an emitter contact region by causing the second conductivity type layer (9) to grow in solid phase.

11. The method as set forth in claim 10 further comprising the steps of:

(e) forming a heavily doped second conductivity type layer (22) buried in a first conductivity type semiconductor substrate (21);
(f) forming a lightly doped second conductivity type epitaxial layer (2) on the heavily doped second conductivity type layer (22) so that the lightly doped second conductivity type epitaxial layer (2) is exposed to a surface of the semiconductor substrate (21); and
(g) forming a heavily doped second conductivity type connection layer (23) for connecting the heavily doped second conductivity type layer (22) to a surface of the semiconductor substrate (21);

the steps (e), (f) and (g) being to be carried out in sequence prior to the step (a), the second conductivity type layer (9) being formed also on the

connection layer (23).

12. The method as set forth in claim 10 or 11, wherein the base region is DC-biased during the step (c).

13. A semiconductor device comprising: (a) a first conductivity type semiconductor substrate (1); (b) a first molecular beam epitaxy layer (4) formed on the semiconductor substrate (1), the first molecular beam epitaxy layer (4) being of a second conductivity type; and (c) a second molecular beam epitaxy layer (9) formed on the first molecular beam epitaxy layer (4), the second molecular beam epitaxy layer (9) being of a first conductivity type, characterized by the step of:

(d) an impurities implantation layer (12) into which first conductivity type impurities are implanted, formed at a surface of the first molecular beam epitaxy layer (4).

14. The semiconductor device as set forth in claim 13 further comprising:

(e) a heavily doped first conductivity type layer (22) buried in the semiconductor substrate (21);
(f) a lightly doped first conductivity type epitaxial layer (2) formed on the heavily doped first conductivity type layer (22) so that the lightly doped first conductivity type epitaxial layer (2) is exposed to a surface of the semiconductor substrate (21); and
(g) a heavily doped first conductivity type connection layer (23) for connecting the heavily doped first conductivity type layer (22) to a surface of the semiconductor substrate (21),

the second molecular beam epitaxy layer being formed also on the connection layer.

15. The semiconductor device as set forth in claim 13 or 14, wherein the first molecular beam epitaxy layer (4) is comprised of an epitaxial layer, and the second molecular beam epitaxy layer (9) is comprised of an amorphous layer.

16. A semiconductor device comprising: (a) a first conductivity type semiconductor substrate (1); (b) a second conductivity type epitaxial layer (4) formed on the semiconductor substrate (1); and (c) a first conductivity type layer (9) formed on the second conductivity type epitaxial layer (4), characterized by:

(d) an impurities implantation layer (12) comprised of a part of the second conductivity type epitaxial layer (4) into which first conductivity type impurities are implanted,

the first conductivity type layer (9) being formed on the impurities implantation layer (12), and being comprised of an amorphous layer.

17. The semiconductor device as set forth in claim 16 further comprising:

(e) a heavily doped first conductivity type layer (22) buried in the semiconductor substrate (21);
(f) a lightly doped first conductivity type epitaxial layer (2) formed on the heavily doped first conductivity type layer (22) so that the lightly doped first conductivity type epitaxial layer (2) is exposed to a surface of the semiconductor substrate (21);
(g) a heavily doped first conductivity type connection layer (23) for connecting the heavily doped first conductivity type layer (22) to a surface of the semiconductor substrate (21),

the first conductivity type layer (9) being formed also on the connection layer (23), and being comprised of an amorphous layer.

18. The semiconductor device as set forth in claim 16 or 17, wherein the impurities are one of antimony (Sb), phosphorus (Pb) and arsenic (As).

19. A semiconductor device comprising: (a) a first conductivity type semiconductor substrate (1); (b) a second conductivity type base region formed in a first conductivity type collector region of the semiconductor substrate (1); and (c) a first conductivity type layer (9) formed on the emitter region, characterized by:

(d) an emitter region formed in the base region, first conductivity type impurities being implanted into the emitter region.

20. The semiconductor device as set forth in claim 19 further comprising:

(e) a heavily doped first conductivity type layer (22) buried in the semiconductor substrate (21);
(f) a lightly doped first conductivity type epitaxial layer (2) formed on the heavily doped first conductivity type layer (22) so that the lightly doped first conductivity type epitaxial layer (2) is exposed to a surface of the semiconductor substrate (21);
(g) a heavily doped first conductivity type connection layer (23) for connecting the heavily doped first conductivity type layer (22) to a surface of the semiconductor substrate (21);

the first conductivity type layer being formed

also on the connection layer, and being comprised of an amorphous layer; and

(h) a collector region formed on the connection layer (23).

21. The semiconductor device as set forth in claim 19 or 20, wherein the base region is composed of epitaxial silicon; and the impurities are one of antimony (Sb), phosphorus (P) and arsenic (As).

FIG.1A
PRIOR ART

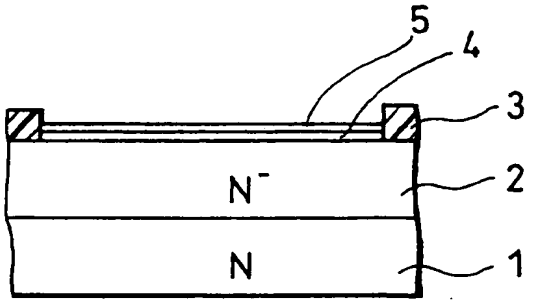

FIG.1B
PRIOR ART

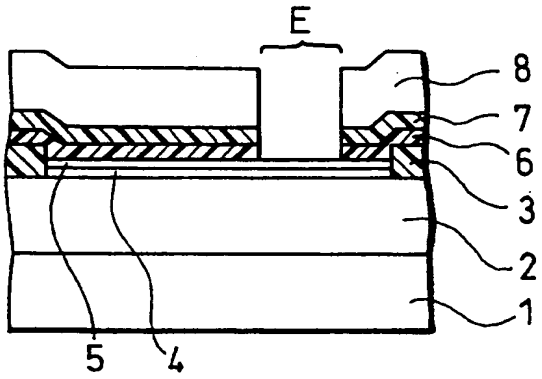

FIG.1C
PRIOR ART

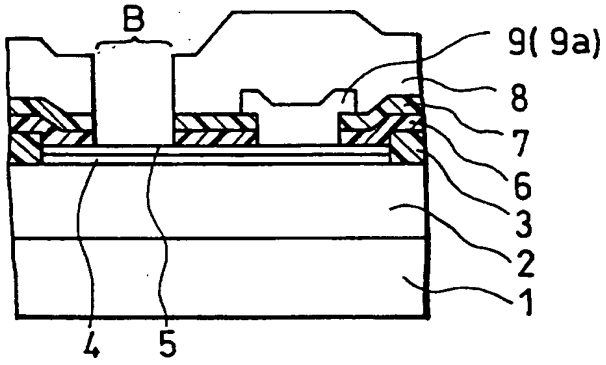

FIG.1D
PRIOR ART

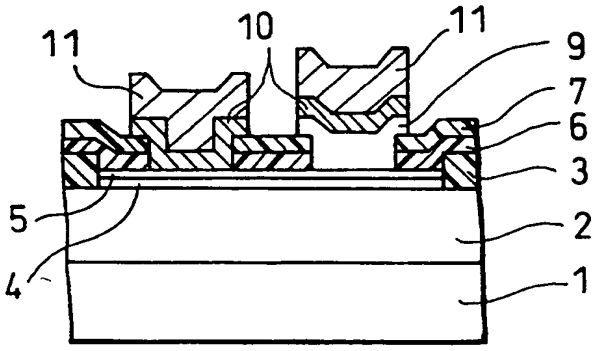

FIG.2
PRIOR ART

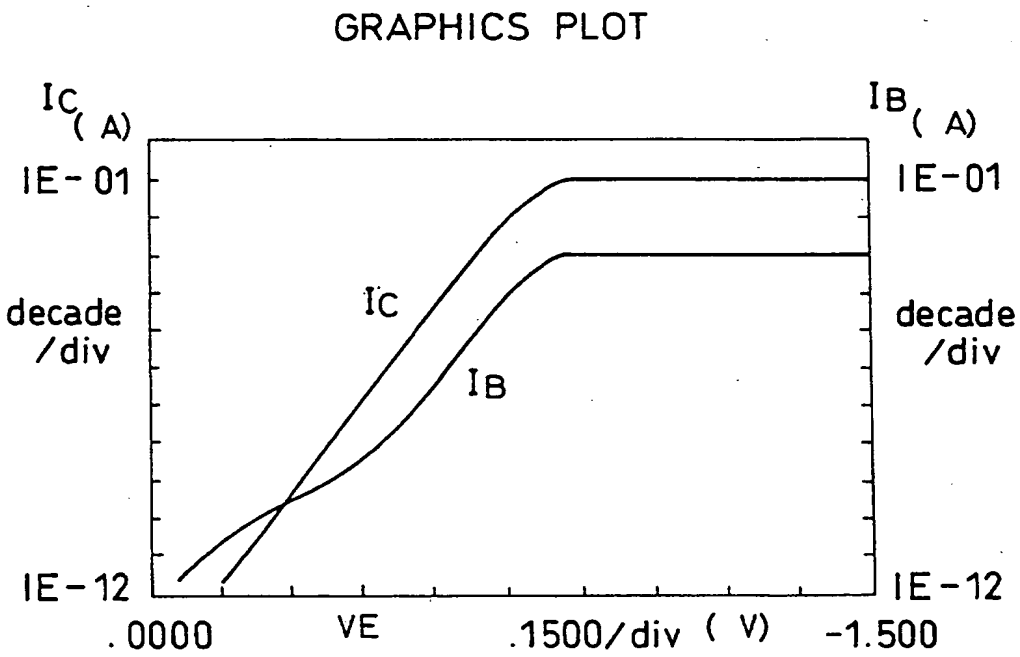

FIG.3

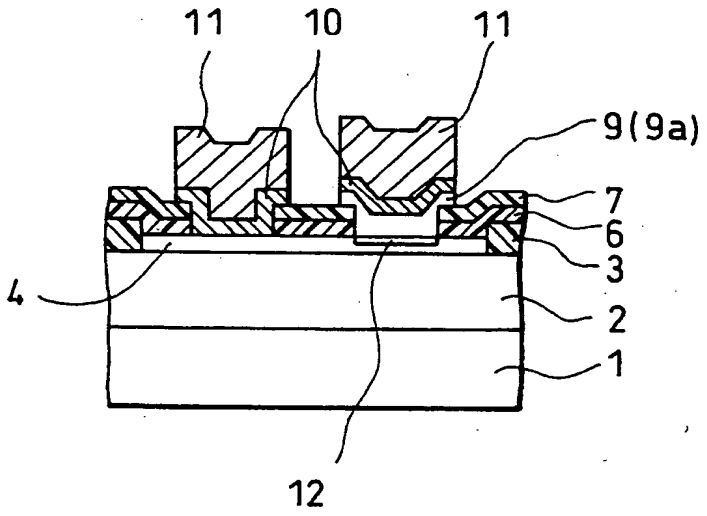

FIG.4A

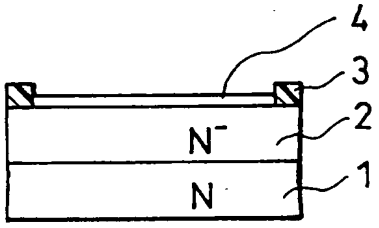

FIG.4B

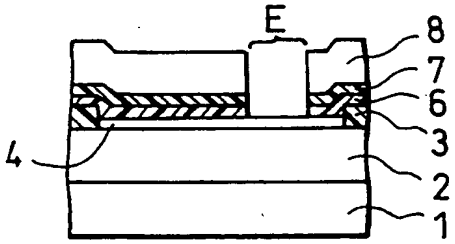

FIG.4C

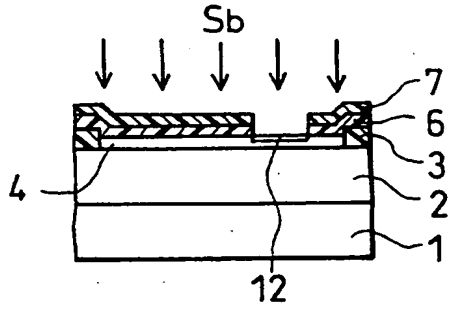

FIG.4D

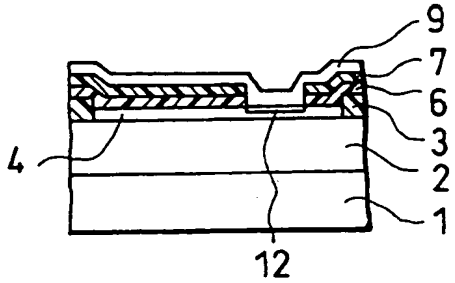

FIG.4E

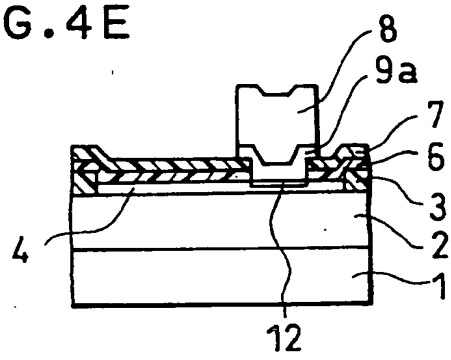

FIG.4F

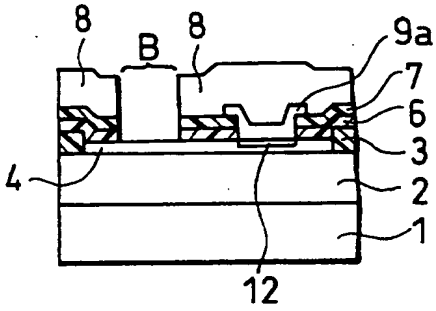

FIG.4G

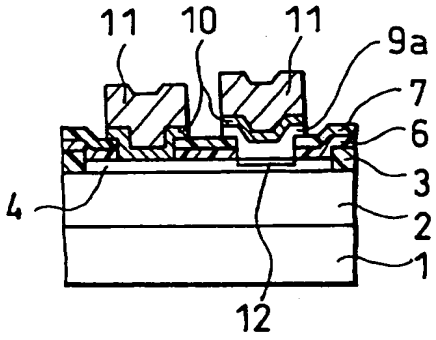

FIG.5

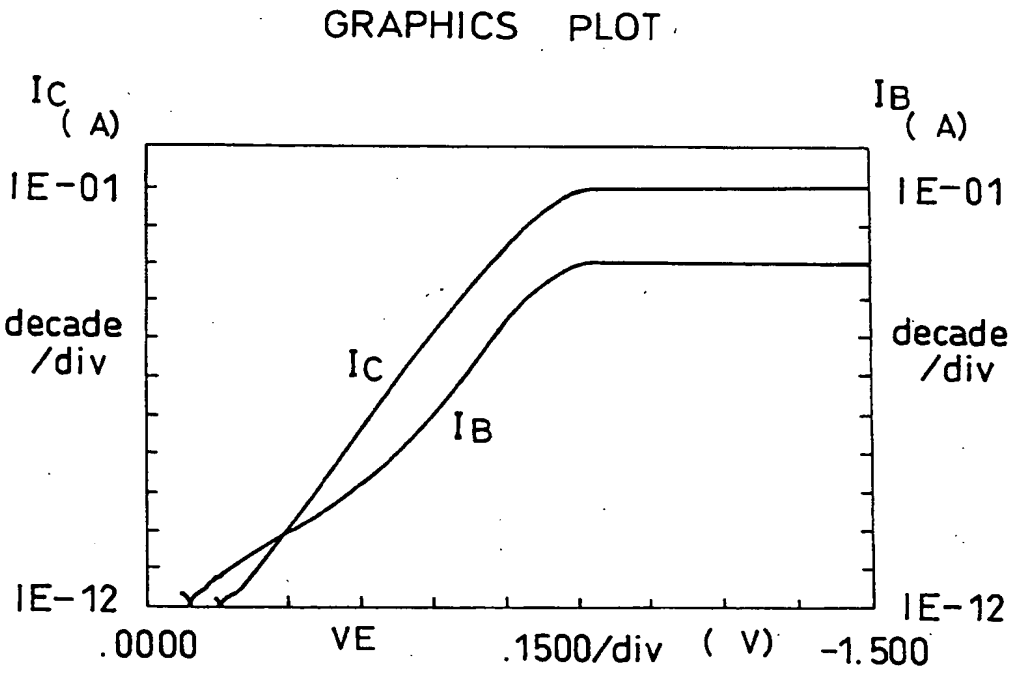
GRAPHICS PLOT
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FIG.6

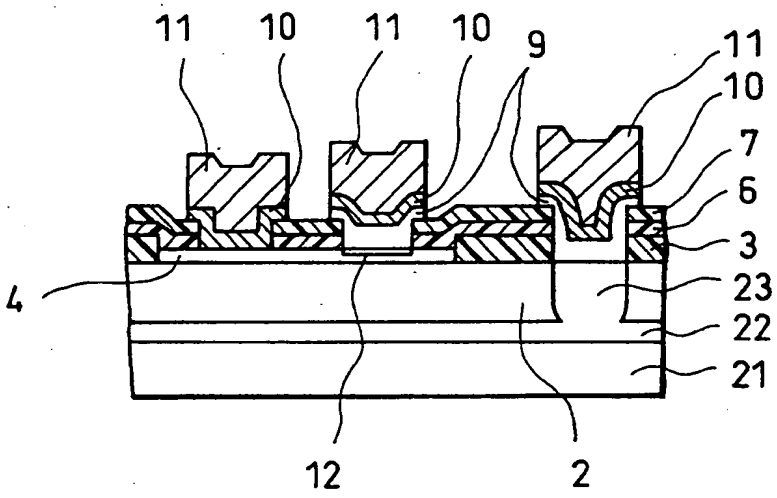

FIG.7A

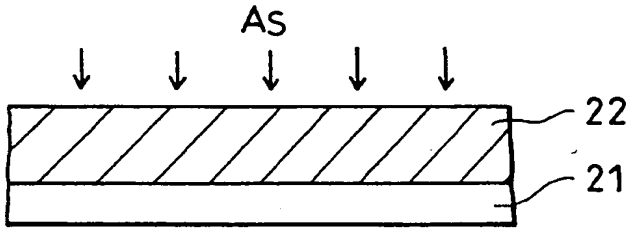

FIG.7B

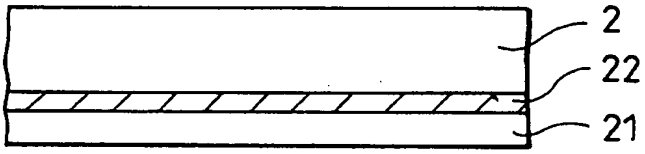

FIG.7C

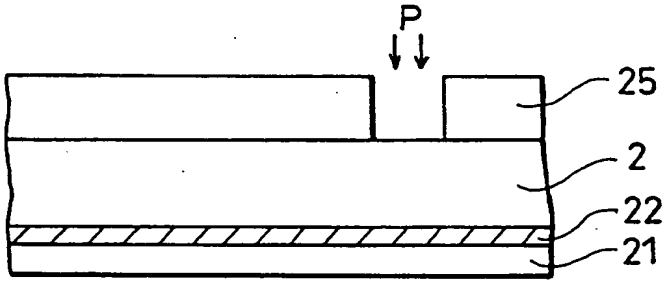

FIG.7D